EAST SEARCH

11/9/2007

L#	Hits	Search String	Databases
S1	566094	(integrated or digital) near2 circuit$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	40	S1 and ((bus near2 (performance or traffic)) with (simulat$3 or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	1665	S1 and (bus with (simulat$3 or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	2232	S1 and (bus near2 (performance or traffic))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	210	S3 and S4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	210	S2 or S5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	23	S6 and (high near2 level near2 language$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	173	S6 and (source$1 or algorithm)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	88	S6 and (source$1 and algorithm)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	27	S6 and (bus with hardware with software)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	156	S6 and (bus with data with transfer$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	8	S6 and (evaluation with function$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	11	S6 and (modif$3 with source$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	1	S6 and ("general purpose" near2 language$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	60	S6 and (architecture with design)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	55	S11 and S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	24	S6 and (bus with process$3 with rate$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	2	S6 and (bus with traffic$3 with rate$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	132	S6 and (bus with traffic$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	11	S6 and (high near2 level near2 design$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	1	S6 and (performance with (feed$3 near2 back))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	1	S6 and ((evaluation or verification) with (feed$3 near2 back))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S23	24	S6 and (feed$3 near2 back)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	1	S6 and (syntax with (correction or analysis))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	103	S7 or S9 or S10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S26	72	S12 or S13 or S16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	7	S17 and S19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	51	S17 or S20 or S23 or S27	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	3687	S3 or S4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	10	S30 and (syntax with (correction or analysis))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	138	S25 or S26 or S28	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	566094	(integrated or digital) near2 circuit$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S33	40	S32 and ((bus near2 (performance or traffic)) with (simulat$3 or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S34	1665	S32 and (bus with (simulat$3 or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S35	2232	S32 and (bus near2 (performance or traffic))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S36	210	S34 and S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S37	210	S33 or S36	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S38	8	S37 and (evaluation with function$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S39	10	S37 and (bus with "data transfer" with evaluation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S40	11	S37 and (high near2 level near2 design$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S41	11	S37 and (modif$3 with source$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S42	24	S37 and (bus with process$3 with rate$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S43	5	S37 and (bus with processing with rate$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S44	3687	S34 or S35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S45	7	S44 and (bus with "processing rate")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S47	3	S44 and (("high level" near2 design$1) with performance)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S46	55	S44 and ("high level" near2 design$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S48	24	S37 and (feed$3 near2 back)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S49	70	S44 and ((bus near2 performance) with (feedback$3 or (feed near2 back)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S50	943	S32 and (bus with simulat$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S51	703	S50 and (source$1 or (programming near2 language$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S52	168	S51 and (bus with (performance or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S53	83	S52 and (hardware with software)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S54	403	S50 and (language$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S55	62	S53 and S54	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S56	1	S50 and ("bus traffic" with (count$3 or increment$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S57	1	S50 and (bus with traffic with (count$3 or increment$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S58	1	S50 and (bus with evaluation with increment$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S59	45	((integrated or digital) near2 circuit$1) with ("architecture design")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S60	4890	((integrated or digital) near2 circuit$1) with simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S62	5	((integrated or digital) near2 circuit$1) with co-simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S63	17	((integrated or digital) near2 circuit$1) same co-simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S64	4939	S59 or S60 or S63	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S65	56	S64 and (bus near2 (traffic or performance or "data trandfer"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S66	161	S64 and ((partition$3 or allocat$3) with (hardware or software))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S67	13	S64 and (bus near2 ((process$3 near2 rate) or rate))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S68	40	S64 and ((algorithm or application) with "source code")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S69	0	S64 and (profil$3 with "source code")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S70	0	S64 and (profil$3 with "data transfer")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S71	117	S64 and (profil$3 with (simulat$3 or bus))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S72	4	S66 and S71	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S73	333	S65 or S66 or S67 or S68 or S71 or S72	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S74	753	((integrated or digital) near2 circuit$1) and ("architecture design")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S75	5612	S64 or S74	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S78	84	S75 and (bus near2 (traffic or performance or "data trandfer"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S79	228	S75 and ((partition$3 or allocat$3) with (hardware or software))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S80	31	S75 and (bus near2 ((process$3 near2 rate) or rate))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S81	71	S75 and ((algorithm or application) with "source code")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S82	0	S75 and (profil$3 with "source code")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S83	1	S75 and (profil$3 with "data transfer")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S84	125	S75 and (profil$3 with (simulat$3 or bus))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S85	7	S79 and S84	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S86	446	S78 or S79 or S80 or S81 or S83 or S84 or S85	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S87	17	S75 and (profil$3 with software)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S88	45	((integrated or digital) near2 circuit$1) with ("architecture design")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S89	4890	((integrated or digital) near2 circuit$1) with simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S90	17	((integrated or digital) near2 circuit$1) same co-simulat$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S91	4939	S88 or S89 or S90	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S92	753	((integrated or digital) near2 circuit$1) and ("architecture design")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S93	5612	S91 or S92	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S94	84	S93 and (bus near2 (traffic or performance or "data trandfer"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S95	228	S93 and ((partition$3 or allocat$3) with (hardware or software))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S96	31	S93 and (bus near2 ((process$3 near2 rate) or rate))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S97	71	S93 and ((algorithm or application) with "source code")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S98	1	S93 and (profil$3 with "data transfer")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S99	125	S93 and (profil$3 with (simulat$3 or bus))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S100	7	S95 and S99	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S101	446	S94 or S95 or S96 or S97 or S98 or S99 or S100	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S102	131	S93 and (bus near2 (traffic or performance or "data transfer"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S103	726060	(integrated or digital) near2 circuit$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S104	51	S103 and ((bus near2 (performance or traffic)) with (simulat$3 or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S105	2194	S103 and (bus with (simulat$3 or evaluat$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S106	3081	S103 and (bus near2 (performance or traffic))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S107	277	S105 and S106	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S108	277	S104 or S107	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S109	201	S108 and ((configur$3 or configuration) with (bus or buss))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S110	5	S108 and ((modifY$3 or modification) with (configur$3 or configuration) with (bus or buss))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S111	17	S108 and ((reconfigur$3 or reconfiguration) with (bus or buss))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S112	55	S108 and ((bus or buss) with bit with line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S113	0	S108 and ((modifY$3 or modification) with (bus or buss) with bit with line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S114	0	S108 and ((modifY$3 or modification) with bit with line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S115	25	S108 and ((modifY$3 or modification) with (bus or buss) with line)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S116	90	S110 or S111 or S112 or S115	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S117	801094	(integrated or digital) near2 circuit$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S119	83	S118 and (co-simulation or cosimulation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S118	2163	S117 and ((partition or partitioned or partitioning) with (hardware or software))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S122	148	S119 or S121	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB
S120	224	S118 and ((bus or buss) with (model or modeled or modeling or simulate or simulated or simulatir	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S121	113	S118 and ((bus or buss) with (simulate or simulated or simulating or simulation))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S123	63	S122 and ((bus or buss) with (traffic or flow or rate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB

09/872,091 **yasuteru Araya et al.**

EAST SEARCH

11/9/2007

Results of search set L29:S25 or S26 or S28

Document	Kind Codes	Title	Issue Date	Current OR	Abstract
US 20050128489	A1	Parametric optimization of optical metrology model	20050616	356/601	
US 20050122500	A1	System and method for lithography simulation	20050609	355/67	
US 20050120327	A1	System and method for lithography simulation	20050602	716/20	

US 20050120012 A1	Adaptive hierarchy usage monitoring HVAC control system	20050602	707/3
US 20050108667 A1	METHOD FOR DESIGNING AN INTEGRATED CIRCUIT HAVING MULTIPLE VOLTAGE DOI	20050519	716/4
US 20050102125 A1	Inter-chip communication system	20050512	703/14
US 20050097500 A1	System and method for lithography simulation	20050505	716/20
US 20050094729 A1	Software and hardware partitioning for multi-standard video compression and decompression	20050505	375/240.16
US 20050091633 A1	System and method for lithography simulation	20050428	716/20
US 20050086565 A1	System and method for generating a test case	20050421	714/741
US 20050081170 A1	Method and apparatus for accelerating the verification of application specific integrated circuit des	20050414	716/6
US 20050081130 A1	Using constrained scan cells to test integrated circuits	20050414	714/726
US 20050076322 A1	System and method for lithography simulation	20050407	716/20
US 20050076282 A1	System and method for testing a circuit design	20050407	714/739
US 20050071706 A1	Slew rate control mechanism	20050331	713/503
US 20050065762 A1	ESD protection device modeling method and ESD simulation method	20050324	703/14
US 20050057748 A1	Selecting a hypothetical profile to use in optical metrology	20050317	356/237.5
US 20050042527 A1	Phase shift mask including sub-resolution assist features for isolated spaces	20050224	430/5
US 20050039156 A1	Design method for essentially digital systems and components thereof and essentially digital syst	20050217	716/18
US 20050025054 A1	Extensible traffic generator for synthesis of network data traffic	20050203	370/235
US 20050015778 A1	Method and system for expressing the algorithms for the manipulation of hardware state using an	20050120	719/321
US 20050004774 A1	Methods and systems for inspection of wafers and reticles using designer intent data	20050106	702/108
US 20040268278 A1	Managing power on integrated circuits using power islands	20041230	716/5
US 20040252701 A1	Systems, processes and integrated circuits for rate and/or diversity adaptation for packet commur	20041216	370/395.21
US 20040250150 A1	Devices, systems and methods for mode driven stops notice	20041209	713/330
US 20040249915 A1	Advanced multi-network client device for wideband multimedia access to private and public wirele	20041209	709/223
US 20040243959 A1	Design method for semiconductor integrated circuit device	20041202	716/7
US 20040236876 A1	Apparatus and method of memory access control for bus masters	20041125	710/22
US 20040236564 A1	Simulation of a PCI device's memory-mapped I/O registers	20041125	703/25
US 20040214150 A1	Interaction education system for teaching patient care	20041028	434/273
US 20040209169 A1	Method of Verifying the Placement of Sub-Resolution Assist Features in a Photomask Layout	20041021	430/5
US 20040204928 A1	Simulator apparatus and related technology	20041014	703/13
US 20040193957 A1	Emulation devices, systems and methods utilizing state machines	20040930	714/30
US 20040193390 A1	Method and apparatus for rapid evaluation of component mismatch in integrated circuit performar	20040930	703/2
US 20040193388 A1	Design time validation of systems	20040930	703/1
US 20040168044 A1	Input pipeline registers for a node in an adaptive computing engine	20040826	712/220
US 20040153301 A1	Integrated circuit development methodology	20040805	703/14
US 20040148151 A1	Model simulation and calibration	20040729	703/22
US 20040145033 A1	Integrated circuit devices and methods and apparatuses for designing integrated circuit devices	20040729	257/659
US 20040136587 A1	Method and device for determining the properties of an integrated circuit	20040715	382/145
US 20040131267 A1	Method and apparatus for performing quality video compression and motion estimation	20040708	382/236
US 20040124874 A1	Apparatus and method for bus signal termination compensation during detected quiet cycle	20040701	326/30
US 20040123256 A1	Software traffic generator/analyser	20040624	716/4
US 20040117756 A1	Methods and apparatuses for designing integrated circuits	20040617	716/18
US 20040098687 A1	System and method for implementing a flexible top level scan architecture using a partitioning alg	20040520	716/7
US 20040088598 A1	Deskew architecture	20040506	713/503
US 20040078767 A1	Representing the design of a sub-module in a hierarchical integrated circuit design and analysis s	20040422	716/8
US 20040054510 A1	System and method for simulating human movement	20040318	703/6
US 20040017575 A1	Optimized model and parameter selection for optical metrology	20040129	356/625

US 20040017574 A1	Model and parameter selection for optical metrology	20040129	356/625
US 20040010650 A1	Configurable multi-port multi-protocol network interface to support packet processing	20040115	710/305
US 20040004216 A1	Test assembly including a test die for testing a semiconductor product die	20040108	257/48
US 20040003362 A1	Timing abstraction and partitioning strategy	20040101	716/6
US 20030229877 A1	System and method for configuring analog elements in a configurable hardware device	20031211	716/16
US 20030229482 A1	Apparatus and method for managing integrated circuit designs	20031211	703/14
US 20030226062 A1	System and method for testing response to asynchronous system errors	20031204	714/38
US 20030225535 A1	Selection of wavelengths for integrated circuit optical metrology	20031204	702/76
US 20030216901 A1	Design apparatus and a method for generating an implementable description of a digital system	20031120	703/13
US 20030214326 A1	Distributed dynamically optimizable processing communications and storage system	20031120	326/101
US 20030212538 A1	Method for full-chip vectorless dynamic IR and timing impact analysis in IC designs	20031113	703/14
US 20030208728 A1	Method and system for simulating resist and etch edges	20031106	716/4
US 20030208350 A1	Facilitating simulation of a model within a distributed environment	20031106	703/22
US 20030204389 A1	Method for numerically simulating an electrical circuit	20031030	703/19
US 20030200425 A1	Devices, systems and methods for mode driven stops	20031023	712/229
US 20030200073 A1	Partitioning a model into a plurality of independent partitions to be processed within a distributed €	20031023	703/17
US 20030196144 A1	Processor condition sensing circuits, systems and methods	20031016	714/34
US 20030192029 A1	System and method for software development	20031009	717/101
US 20030188299 A1	Method and apparatus for simulation system compiler	20031002	717/141
US 20030187853 A1	Distributed data storage system and method	20031002	707/10
US 20030187840 A1	Metrology diffraction signal adaptation for tool-to-tool matching	20031002	707/4
US 20030187602 A1	METROLOGY HARDWARE SPECIFICATION USING A HARDWARE SIMULATOR	20031002	702/94
US 20030163295 A1	Generation and use of integrated circuit profile-based simulation information	20030828	703/14
US 20030149954 A1	Methods and apparatuses for designing integrated circuits	20030807	716/18
US 20030144828 A1	Hub array system and method	20030731	703/21
US 20030142819 A1	Device and method for evaluating algorithms	20030731	380/28
US 20030142726 A1	Universal rake receiver	20030731	375/146
US 20030139956 A1	Methods and systems for role analysis	20030724	705/7
US 20030128140 A1	Code compression algorithms and architectures for embedded systems	20030710	341/107
US 20030126059 A1	Intelectual property (IP) brokering system and method	20030703	705/36R
US 20030125923 A1	Simulation of di/dt-induced power supply voltage variation	20030703	703/20
US 20030125922 A1	Mechanism for estimating and controlling di/dt-induced power supply voltage variations	20030703	703/18
US 20030093764 A1	Automated system-on-chip integrated circuit design verification system	20030515	716/5
US 20030093255 A1	Hot plug and hot pull system simulation	20030515	703/13
US 20030093252 A1	Message packet logging in a distributed simulation system	20030515	703/13
US 20030088840 A1	Method of designing semiconductor integrated circuit device, method of analyzing power consum	20030508	716/7
US 20030079195 A1	Methods and apparatuses for designing integrated circuits	20030424	716/8
US 20030079132 A1	Computer functional architecture and a locked down environment in a client-server architecture	20030424	713/182
US 20030075765 A1	Semiconductor integrated circuit	20030424	257/393
US 20030073060 A1	Interactive education system for teaching patient care	20030417	434/262
US 20030037305 A1	Method and apparatus for evaluating logic states of design nodes for cycle-based simulation	20030220	716/4
US 20030018461 A1	Simulation monitors based on temporal formulas	20030123	703/14
US 20030016461 A1	Systems, apparatus, and methods to determine thermal decay characterization from an equalized	20030123	360/25
US 20030013024 A1	Phase shift mask including sub-resolution assist features for isolated spaces	20030116	430/5
US 20030009734 A1	Method for generating design constraints for modules in a hierarchical integrated circuit design sy	20030109	716/6
US 20030008222 A1	Phase shift mask layout process for patterns including intersecting line segments	20030109	430/5

US 20030005263 A1	Shared resource queue for simultaneous multithreaded processing	20030102	712/218
US 20020197546 A1	Phase shift masking for "double-T" intersecting lines	20021226	430/5
US 20020194572 A1	Methods and apparatuses for designing integrated circuits	20021219	716/1
US 20020186721 A1	Methods and systems for monitoring traffic received from and loading simulated traffic on broadb	20021212	370/522
US 20020152060 A1	Inter-chip communication system	20021017	703/17
US 20020149598 A1	Method and apparatus for adjusting subpixel intensity values based upon luminance characteristi	20021017	345/589
US 20020147875 A1	Response and data phases in a highly pipelined bus architecture	20021010	710/305
US 20020144247 A1	Method and apparatus for simultaneous optimization of code targeting multiple machines	20021003	717/155
US 20020144212 A1	System, method and computer program product for web-based integrated circuit design	20021003	716/1
US 20020144183 A1	Microprocessor design support for computer system and platform validation	20021003	714/37
US 20020138814 A1	Virtual component having a detachable verification-supporting circuit, a method of verifying the sa	20020926	716/5
US 20020133785 A1	Semiconductor integrated circuit manufacturing method and model parameter extracting method,	20020919	716/1
US 20020133325 A1	Discrete event simulator	20020919	703/17
US 20020124234 A1	Method for designing circuits with sections having different supply voltages	20020905	716/18
US 20020124085 A1	Method of simulating operation of logical unit, and computer-readable recording medium retaining	20020905	709/226
US 20020123872 A1	Method and apparatus for simulating manufacturing, electrical and physical characteristics of a s	20020905	703/15
US 20020108092 A1	Digital circuit design method using programming language	20020808	716/1
US 20020097216 A1	Animated video device with synchronized voice	20020725	345/108
US 20020095304 A1	System, method, and apparatus for storing emissions and susceptibility information	20020718	705/1
US 20020087940 A1	Method for designing large standard-cell based integrated circuits	20020704	716/2
US 20020087939 A1	Method for designing large standard-cell based integrated circuits	20020704	716/2
US 20020066082 A1	Bus performance evaluation method for algorithm description	20020530	717/135
US 20020059554 A1	Design method for semiconductor integrated circuit device	20020516	716/8
US 20020059501 A1	High-availability super server	20020516	711/144
US 20020040466 A1	Automated EMC-driven layout and floor planning of electronic devices and systems	20020404	716/9
US 20020039030 A1	System, method, and apparatus for product diagnostic and evaluation testing	20020404	324/750
US 20020038401 A1	Design tool for systems-on-a-chip	20020328	710/305
US 20020033706 A1	System method, and apparatus for field scanning	20020321	324/750
US 20020023252 A1	METHOD FOR INCREMENTAL TIMING ANALYSIS	20020221	716/6
US 20020022951 A1	Method, apparatus and computer program product for determination of noise in mixed signal syst	20020221	703/16
US 20020019969 A1	Hardware and software co-simulation including simulating the cache of a target processor	20020214	716/5
US 20020016704 A1	Adjoint sensitivity determination for nonlinear circuit models	20020207	703/14
US 20020016674 A1	Golf course yardage and information system having improved zone information and display chara	20020207	701/215
US 20020013918 A1	Devices, systems and methods for mode driven stops	20020131	714/30
US 20020011949 A1	Golf course yardage and information system with zone detection	20020131	342/357.06
US 20020010544 A1	Display monitor for golf cart yardage and information system	20020124	701/213
US 20020004927 A1	Method for designing ingegrated circuit	20020110	716/2
US 20010056341 A1	Method and apparatus for debugging programs in a distributed environment	20011227	703/22
US 20010049593 A1	Software tool to allow field programmable system level devices	20011206	703/14
US 20010039640 A1	Method and apparatus for wiring integrated circuits with multiple power buses based on performa	20011108	716/2
US 20010037424 A1	Snoop phase in a highly pipelined bus architecture	20011101	710/220
US 20010037421 A1	Enhanced highly pipelined bus architecture	20011101	710/305
US 20010029601 A1	Semiconductor device analyzer, method for analyzing/manufacturing semiconductor device, and s	20011011	716/19
US 20010012014 A1	SINGLE LOGICAL IN X WINDOWS WITH DIRECT HARDWARE ACCESS TO THE FRAME I	20010809	345/541
US 20010011212 A1	METHOD AND APPARATUS FOR GATE-LEVEL SIMULATION OF SYNTHESIZED REGISTE	20010802	703/22
US 6907487 B2	Enhanced highly pipelined bus architecture	20050614	710/305

US 6892362 B1	Hybrid state machine	20050510	716/1
US 6891626 B2	Caching of intra-layer calculations for rapid rigorous coupled-wave analyses	20050510	356/625
US 6885946 B1	Method and apparatus for performing image process of seismic data	20050426	702/16
US 6880031 B2	Snoop phase in a highly pipelined bus architecture	20050412	710/305
US 6873720 B2	System and method of providing mask defect printability analysis	20050329	382/149
US 6871298 B1	Method and apparatus that simulates the execution of paralled instructions in processor functiona	20050322	714/33
US 6859831 B1	Method and apparatus for internetworked wireless integrated network sensor (WINS) nodes	20050222	709/224
US 6854048 B1	Speculative execution control with programmable indicator and deactivation of multiaccess recove	20050208	712/216
US 6846120 B2	System for printing information on a mailing medium	20050125	400/611
US 6845494 B2	Method for generating design constraints for modules in a hierarchical integrated circuit design sy	20050118	716/6
US 6845489 B1	Database for design of integrated circuit device and method for designing integrated circuit device	20050118	716/1
US 6842714 B1	Method for determining the leakage power for an integrated circuit	20050111	702/136
US 6842035 B2	Apparatus and method for bus signal termination compensation during detected quiet cycle	20050111	326/30
US 6834380 B2	Automated EMC-driven layout and floor planning of electronic devices and systems	20041221	716/10
US 6834375 B1	System and method for product yield prediction using a logic characterization vehicle	20041221	716/2
US 6832251 B1	Method and apparatus for distributed signal processing among internetworked wireless integrated	20041214	709/224
US 6826607 B1	Apparatus for internetworked hybrid wireless integrated network sensors (WINS)	20041130	709/224
US 6826517 B2	Method and apparatus for simulating manufacturing, electrical and physical characteristics of a se	20041130	703/2
US 6825052 B2	Test assembly including a test die for testing a semiconductor product die	20041130	438/15
US 6811935 B2	Phase shift mask layout process for patterns including intersecting line segments	20041102	430/5
US 6810442 B1	Memory mapping system and method	20041026	710/22
US 6810372 B1	Multimodal optimization technique in test generation	20041026	703/13
US 6804735 B2	Response and data phases in a highly pipelined bus architecture	20041012	710/112
US 6801220 B2	Method and apparatus for adjusting subpixel intensity values based upon luminance characteristic	20041005	345/694
US 6792563 B1	Method and apparatus for bus activity tracking	20040914	714/43
US 6792328 B2	Metrology diffraction signal adaptation for tool-to-tool matching	20040914	700/121
US 6785876 B2	Design method for semiconductor integrated circuit device	20040831	716/7
US 6785873 B1	Emulation system with multiple asynchronous clocks	20040831	716/4
US 6779157 B2	Semiconductor integrated circuit manufacturing method and model parameter extracting method,	20040817	716/2
US 6777141 B2	Phase shift mask including sub-resolution assist features for isolated spaces	20040817	430/5
US 6766419 B1	Optimization of cache evictions through software hints	20040720	711/133
US 6760866 B2	Process of operating a processor with domains and clocks	20040706	714/34
US 6760478 B1	Method and apparatus for performing two pass quality video compression through pipelining and l	20040706	382/236
US 6758676 B2	Interactive education system for teaching patient care	20040706	434/262
US 6757645 B2	Visual inspection and verification system	20040629	703/13
US 6754763 B2	Multi-board connection system for use in electronic design automation	20040622	710/317
US 6751583 B1	Hardware and software co-simulation including simulating a target processor using binary translat	20040615	703/17
US 6742165 B2	System, method and computer program product for web-based integrated circuit design	20040525	716/1
US 6735743 B1	Method and apparatus for invalid state detection	20040511	716/4
US 6735630 B1	Method for collecting data using compact internetworked wireless integrated network sensors (WI	20040511	709/224
US 6734509 B2	Semiconductor integrated circuit	20040511	257/393
US 6732350 B1	Local naming for HDL compilation	20040504	716/18
US 6721691 B2	Metrology hardware specification using a hardware simulator	20040413	702/189
US 6718429 B1	Configurable register file with multi-range shift register support	20040406	711/101
US 6711729 B1	Methods and apparatuses for designing integrated circuits using automatic reallocation technique	20040323	716/18
US 6704895 B1	Integrated circuit with emulation register in JTAG JAP	20040309	714/726

US 6697773 B1	Using assignment decision diagrams with control nodes for sequential review during behavioral si	20040224	703/15
US 6694488 B1	System for the design of high-performance communication architecture for system-on-chips using	20040217	716/1
US 6675139 B1	Floor plan-based power bus analysis and design tool for integrated circuits	20040106	703/17
US 6671818 B1	Problem isolation through translating and filtering events into a standard object format in a networl	20031230	714/4
US 6668364 B2	Methods and apparatuses for designing integrated circuits	20031223	716/7
US 6668356 B2	Method for designing circuits with sections having different supply voltages	20031223	716/1
US 6668337 B2	Method for designing integrated circuit based on the transaction analyzing model	20031223	714/6
US 6658633 B2	Automated system-on-chip integrated circuit design verification system	20031202	716/5
US 6651225 B1	Dynamic evaluation logic system and method	20031118	716/4
US 6640249 B1	Presentation services patterns in a netcentric environment	20031028	709/228
US 6640248 B1	Application-aware, quality of service (QoS) sensitive, media access control (MAC) layer	20031028	709/226
US 6640244 B1	Request batcher in a transaction services patterns environment	20031028	709/207
US 6640238 B1	Activity component in a presentation services patterns environment	20031028	709/201
US 6636242 B2	View configurer in a presentation services patterns environment	20031021	715/764
US 6629296 B1	Functional verification of integrated circuit designs	20030930	716/5
US 6624078 B1	Methods for analyzing the effectiveness of wafer backside cleaning	20030923	438/692
US 6615389 B1	Database for designing integrated circuit device, and method for designing integrated circuit devic	20030902	716/1
US 6615253 B1	Efficient server side data retrieval for execution of client side applications	20030902	709/219
US 6615199 B1	Abstraction factory in a base services pattern environment	20030902	706/50
US 6610449 B2	Phase shift masking for "double-T" intersecting lines	20030826	430/5
US 6606744 B1	Providing collaborative installation management in a network-based supply chain environment	20030812	717/174
US 6606721 B1	Method and apparatus that tracks processor resources in a dynamic pseudo-random test progran	20030812	714/728
US 6606660 B1	Stream-based communication in a communication services patterns environment	20030812	709/227
US 6606609 B1	Apparatus and method for operating an integrated circuit	20030812	706/1
US 6606588 B1	Design apparatus and a method for generating an implementable description of a digital system	20030812	703/15
US 6604230 B1	Multi-logic device systems having partial crossbar and direct interconnection architectures	20030805	716/16
US 6601234 B1	Attribute dictionary in a business logic services environment	20030729	717/108
US 6601192 B1	Assertion component in environment services patterns	20030729	714/38
US 6578188 B1	Method and apparatus for a network-based mask defect printability analysis system	20030610	716/19
US 6578187 B2	Digital circuit design method using programming language	20030610	716/18
US 6578068 B1	Load balancer in environment services patterns	20030610	709/203
US 6571282 B1	Block-based communication in a communication services patterns environment	20030527	709/219
US 6567967 B2	Method for designing large standard-cell base integrated circuits	20030520	716/10
US 6551844 B1	Test assembly including a test die for testing a semiconductor product die	20030422	438/14
US 6550057 B1	Piecemeal retrieval in an information services patterns environment	20030415	717/126
US 6549949 B1	Fixed format stream in a communication services patterns environment	20030415	709/236
US 6546505 B1	Processor condition sensing circuits, systems and methods	20030408	714/30
US 6541165 B1	Phase shift mask sub-resolution assist features	20030401	430/5
US 6539522 B1	Method of developing re-usable software for efficient verification of system-on-chip integrated circ	20030325	716/5
US 6539497 B2	IC with selectively applied functional and test clocks	20030325	714/30
US 6539396 B1	Multi-object identifier system and method for information service pattern environment	20030325	707/103R
US 6529948 B1	Multi-object fetch component	20030304	709/217
US 6529909 B1	Method for translating an object attribute converter in an information services patterns environmer	20030304	707/10
US 6526462 B1	Programmable multi-tasking memory management system	20030225	710/242
US 6525690 B2	Golf course yardage and information system with zone detection	20030225	342/357.13
US 6524752 B1	Phase shift masking for intersecting lines	20030225	430/5

US 6523157 B1	Method for designing integrated circuit device and database for design of integrated circuit device	20030218	716/10
US 6522985 B1	Emulation devices, systems and methods utilizing state machines	20030218	702/117
US 6519754 B1	Methods and apparatuses for designing integrated circuits	20030211	716/18
US 6519742 B1	Local naming for HDL compilation	20030211	716/3
US 6513146 B1	Method of designing semiconductor integrated circuit device, method of analyzing power consum	20030128	716/7
US 6505147 B1	Method for process simulation	20030107	703/2
US 6503666 B1	Phase shift masking for complex patterns	20030107	430/5
US 6503087 B1	Interactive education system for teaching patient care	20030107	434/262
US 6502213 B1	System, method, and article of manufacture for a polymorphic exception handler in environment s	20021231	714/49
US 6496850 B1	Clean-up of orphaned server contexts	20021217	709/203
US 6493863 B1	Method of designing semiconductor integrated circuit	20021210	716/18
US 6493784 B1	Communication device, multiple bus control device and LSI for controlling multiple bus	20021210	710/309
US 6490642 B1	Locked read/write on separate address/data bus using write barrier	20021203	710/110
US 6487701 B1	System and method for AC performance tuning by thereshold voltage shifting in tubbed semiconc	20021126	716/4
US 6484305 B1	Impurity quantity transfer device enabling reduction in pseudo diffusion error generated at integral	20021119	716/20
US 6484304 B1	Method of generating application specific integrated circuits using a programmable hardware arch	20021119	716/18
US 6477665 B1	System, method, and article of manufacture for environment services patterns in a netcentic envir	20021105	714/39
US 6477580 B1	Self-described stream in a communication services patterns environment	20021105	709/231
US 6470489 B1	Design rule checking system and method	20021022	716/21
US 6470482 B1	METHOD AND SYSTEM FOR CREATING, DERIVING AND VALIDATING STRUCTURAL DE	20021022	716/6
US 6470242 B1	Display monitor for golf cart yardage and information system	20021022	701/1
US 6467003 B1	Fault tolerant data communication network	20021015	710/117
US 6457089 B1	Microprocessor bus structure	20020924	710/306
US 6453452 B1	Method and apparatus for data hierarchy maintenance in a system for mask description	20020917	716/8
US 6449761 B1	Method and apparatus for providing multiple electronic design solutions	20020910	716/11
US 6446239 B1	Method and apparatus for optimizing electronic design	20020903	716/2
US 6442748 B1	System, method and article of manufacture for a persistent state and persistent object separator i	20020827	717/108
US 6438735 B1	Methods and apparatuses for designing integrated circuits	20020820	716/7
US 6438594 B1	Delivering service to a client via a locally addressable interface	20020820	709/225
US 6434628 B1	Common interface for handling exception interface name with additional prefix and suffix for hand	20020813	714/48
US 6434568 B1	Information services patterns in a netcentric environment	20020813	707/103R
US 6429029 B1	Concurrent design and subsequent partitioning of product and test die	20020806	438/14
US 6427226 B1	Selectively reducing transistor channel length in a semiconductor device	20020730	716/10
US 6427224 B1	Method for efficient verification of system-on-chip integrated circuit designs including an embedde	20020730	716/4
US 6421251 B1	Array board interconnect system and method	20020716	361/788
US 6417849 B2	Single logical screen in X windows with direct hardware access to the frame buffer for 3D renderi	20020709	345/419
US 6412101 B1	Simultaneous path optimization (SPO) system and method	20020625	716/10
US 6389586 B1	Method and apparatus for invalid state detection	20020514	716/18
US 6389577 B1	Analyzing CMOS circuit delay	20020514	716/4
US 6389498 B1	Microprocessor having addressable communication port	20020514	710/268
US 6389379 B1	Converification system and method	20020514	703/14
US 6370679 B1	Data hierarchy layout correction and verification method and apparatus	20020409	716/19
US 6370492 B1	Modified design representation for fast fault simulation of an integrated circuit	20020409	703/13
US 6367056 B1	Method for incremental timing analysis	20020402	716/5
US 6356945 B1	Method and apparatus including system architecture for multimedia communications	20020312	709/231
US 6349392 B1	Devices, systems and methods for mode driven stops	20020219	714/30

US 6339836 B1	Automated design partitioning	20020115	716/5
US 6336087 B1	Method and apparatus for gate-level simulation of synthesized register transfer level design with s	20020101	703/15
US 6324678 B1	Method and system for creating and validating low level description of electronic design	20011127	716/18
US 6321366 B1	Timing-insensitive glitch-free logic system and method	20011120	716/6
US 6314552 B1	Electronic design creation through architectural exploration	20011106	716/18
US 6311310 B1	Method and apparatus for wiring integrated circuits with multiple power buses based on performai	20011030	716/2
US 6311147 B1	Integrated circuit power net analysis	20011030	703/18
US 6311146 B1	Circuit simulation with improved circuit partitioning	20011030	703/14
US 6305006 B1	Generating candidate architectures for an architectural exploration based electronic design creatic	20011016	716/18
US 6304834 B1	Method and apparatus for semiconductor device simulation with linerly changing quasi-fermi potei	20011016	703/4
US 6295546 B1	Method and apparatus for eliminating the transpose buffer during a decomposed forward or inver:	20010925	708/402
US 6295517 B1	Method and apparatus for adaptively or selectively choosing event-triggered cycle-based simulatic	20010925	703/15
US 6292589 B1	Method for choosing rate control parameters in motion-compensated transform-based picture cod	20010918	382/239
US 6285970 B1	Computer simulation method of silicon oxidation	20010904	703/2
US 6272451 B1	Software tool to allow field programmable system level devices	20010807	703/13
US 6263484 B1	Prototyping system and a method of operating the same	20010717	716/18
US 6240376 B1	Method and apparatus for gate-level simulation of synthesized register transfer level designs with	20010529	703/15
US 6240375 B1	Method of simulating an integrated circuit for error correction in a configuration model, and a com	20010529	703/14
US 6236940 B1	Display monitor for golf cart yardage and information system	20010522	701/300
US 6236360 B1	Golf course yardage and information system	20010522	342/357.13
US 6233540 B1	Design environment and a method for generating an implementable description of a digital systerr	20010515	703/14
US 6233361 B1	Topography processor system	20010515	382/260
US 6216252 B1	Method and system for creating, validating, and scaling structural description of electronic device	20010410	716/1
US 6212493 B1	Profile directed simulation used to target time-critical crossproducts during random vector testing	20010403	703/22
US 6212487 B1	Method and apparatus of establishing a region to be made amorphous	20010403	703/12
US 6208954 B1	Method for scheduling event sequences	20010327	703/16
US 6195790 B1	Electrical parameter evaluation system, electrical parameter evaluation method, and computer-rea	20010227	716/20
US 6193152 B1	Modular signature and data-capture system and point of transaction payment and reward system	20010227	235/380
US 6191663 B1	Echo reduction on bit-serial, multi-drop bus	20010220	333/17.3
US 6178533 B1	Method and system for design verification	20010123	714/739
US 6173240 B1	Multidimensional uncertainty analysis	20010109	703/2
US 6167491 A	High performance digital electronic system architecture and memory circuit therefor	20001226	711/149
US 6150724 A	Multi-chip semiconductor device and method for making the device by using multiple flip chip inte	20001121	257/777
US 6134516 A	Simulation server system and method	20001017	703/27
US 6128718 A	Apparatus and method for a base address register on a computer peripheral device supporting cc	20001003	711/212
US 6117182 A	Optimum buffer placement for noise avoidance	20000912	716/8
US 6101276 A	Method and apparatus for performing two pass quality video compression through pipelining and l	20000808	382/236
US 6085336 A	Data processing devices, systems and methods with mode driven stops	20000704	714/30
US 6078745 A	Method and apparatus for size optimization of storage units	20000620	717/151
US 6072994 A	Digitally programmable multifunction radio system architecture	20000606	455/84
US 6067041 A	Moving target simulator	20000523	342/171
US 6061222 A	Method and apparatus for reducing noise in integrated circuit chips	20000509	361/111
US 6052706 A	Apparatus for performing fast multiplication	20000418	708/631
US 6038383 A	Method and apparatus for determining signal line interconnect widths to ensure electromigration r	20000314	716/5
US 6032268 A	Processor condition sensing circuits, systems and methods	20000229	714/30
US 6026230 A	Memory simulation system and method	20000215	703/13

US 6026217 A	Method and apparatus for eliminating the transpose buffer during a decomposed forward or inver	20000215	709/247
US 6023573 A	Apparatus and method for analyzing circuits using reduced-order modeling of large linear subcirc	20000208	703/2
US 6021266 A	Method of designing an integrated circuit using scheduling and allocation with parallelism and har	20000201	716/2
US 6014570 A	Efficient radio signal diversity combining using a small set of discrete amplitude and phase weigh	20000111	455/500
US 6009256 A	Simulation/emulation system and method	19991228	703/13
US 6009255 A	Method of deposition profile simulation	19991228	703/6
US 6002861 A	Method for performing simulation using a hardware emulation system	19991214	703/16
US 5995080 A	Method and apparatus for interleaving and de-interleaving YUV pixel data	19991130	345/603
US 5991863 A	Single carry/borrow propagate adder/decrementer for generating register stack addresses in a mi	19991123	711/219
US 5991533 A	Verification support system	19991123	703/28
US 5966312 A	Method for monitoring and analyzing manufacturing processes using statistical simulation with sir	19991012	703/6
US 5949994 A	Dedicated context-cycling computer with timed context	19990907	712/228
US 5937179 A	Integrated circuit design system with shared hardware accelerator and processes of designing int	19990810	716/16
US 5933356 A	Method and system for creating and verifying structural logic model of electronic design from beh	19990803	703/15
US 5911059 A	Method and apparatus for testing software	19990608	703/23
US 5910897 A	Specification and design of complex digital systems	19990608	716/19
US 5907853 A	Method and apparatus for maintaining duplicate cache tags with selectable width	19990525	711/3
US 5907698 A	Method and apparatus for characterizing static and dynamic operation of an architectural system	19990525	716/6
US 5889687 A	Simulator, simulation and fabrication methods of semiconductor device and storage medium stori	19990330	703/4
US 5886909 A	Defect diagnosis using simulation for IC yield improvement	19990323	716/4
US 5884062 A	Microprocessor with pipeline status integrity logic for handling multiple stage writeback exceptions	19990316	712/218
US 5880971 A	Methodology for deriving executable low-level structural descriptions and valid physical implement	19990309	716/6
US 5880967 A	Minimization of circuit delay and power through transistor sizing	19990309	716/6
US 5878369 A	Golf course yardage and information system	19990302	701/215
US 5870308 A	Method and system for creating and validating low-level description of electronic design	19990209	716/18
US 5867399 A	System and method for creating and validating structural description of electronic system from hig	19990202	716/18
US 5867397 A	Method and apparatus for automated design of complex structures using genetic programming	19990202	703/14
US 5862149 A	Method of partitioning logic designs for automatic test pattern generation based on logical register	19990119	714/726
US 5841670 A	Emulation devices, systems and methods with distributed control of clock domains	19981124	703/23
US 5825680 A	Method and apparatus for performing fast division	19981020	708/650
US 5822579 A	Microprocessor with dynamically controllable microcontroller condition selection	19981013	712/245
US 5812414 A	Method for performing simulation using a hardware logic emulation system	19980922	716/16
US 5805792 A	Emulation devices, systems, and methods	19980908	714/28
US 5802580 A	High performance digital electronic system architecture and memory circuit thereof	19980901	711/149
US 5801958 A	Method and system for creating and validating low level description of electronic design from high	19980901	716/18
US 5796623 A	Apparatus and method for performing computations with electrically reconfigurable logic devices	19980818	703/23
US 5774738 A	State machines	19980630	712/1
US 5764951 A	Methods for automatically pipelining loops	19980609	716/1
US 5764234 A	Trapezoidal partitioning method and apparatus therefor	19980609	345/423
US 5758123 A	Verification support system	19980526	703/22
US 5748872 A	Direct replacement cell fault tolerant architecture	19980505	714/11
US 5734581 A	Method for implementing tri-state nets in a logic emulation system	19980331	703/15
US 5719796 A	System for monitoring and analyzing manufacturing processes using statistical simulation with sir	19980217	703/13
US 5712806 A	Optimized multiplexer structure for emulation systems	19980127	716/16
US 5706290 A	Method and apparatus including system architecture for multimedia communication	19980106	370/465
US 5694481 A	Automated design analysis system for generating circuit schematics from high magnification imag	19971202	382/145

US 5692160 A	Temperature, process and voltage variant slew rate based power usage simulation and method	19971125	703/23
US 5689431 A	Golf course yardage and information system	19971118	701/213
US 5678028 A	Hardware-software debugger using simulation speed enhancing techniques including skipping ur	19971014	703/22
US 5673199 A	Computer aided reuse tool	19970930	703/1
US 5663900 A	Electronic simulation and emulation system	19970902	716/17
US 5661662 A	Structures and methods for adding stimulus and response functions to a circuit design undergoin	19970826	716/16
US 5657241 A	Routing methods for use in a logic emulation system	19970812	716/16
US 5625803 A	Slew rate based power usage simulation and method	19970429	703/14
US 5625580 A	Hardware modeling system and method of use	19970429	703/21
US 5623418 A	System and method for creating and validating structural description of electronic system	19970422	716/1
US 5621652 A	System and method for verifying process models in integrated circuit process simulators	19970415	716/5

Interference checked

09/872,091 yasuteru Araya et al.

EAST SEARCH

11/9/2007

L#	Hits	Search String	Databases
L1	18	((integrated or digital) near2 circuit$1) with ("architecture design")	US-PGPUB
L2	9	((integrated or digital) near2 circuit$1) with ("architectural design")	US-PGPUB
L3	1832	((integrated or digital) near2 circuit$1) with simulat$3	US-PGPUB
L4	16	((integrated or digital) near2 circuit$1) same co-simulat$3	US-PGPUB
L5	1865	1 or 2 or 3 or 4	US-PGPUB
L6	389	((integrated or digital) near2 circuit$1) and ("architecture design")	US-PGPUB
L7	168	((integrated or digital) near2 circuit$1) and ("architectural design")	US-PGPUB
L8	2353	5 or 6 or 7	US-PGPUB
L9	68	8 and (bus near2 (traffic or performance or "data transfer"))	US-PGPUB
L10	125	8 and ((partition$3 or allocat$3) with (hardware or software))	US-PGPUB
L11	21	8 and (bus near2 ((process$3 near2 rate) or rate))	US-PGPUB
L12	31	8 and ((algorithm or application) with "source code")	US-PGPUB
L14	8	8 and (profil$3 with "data transfer")	US-PGPUB
L15	82	8 and (profil$3 with (simulat$3 or bus))	US-PGPUB
L16	7	10 and 15	US-PGPUB

09/872,091 yasuteru Araya et al.

EAST SEARCH

11/9/2007

Results of search set L29:S25 or S26 or S28

Document Kind Codes	Title	Issue Date	Current OR	Abstract
US 20070260949 A1	Trading propensity-based clustering of circuit elements in a circuit design	20071108	714/726	
US 20070245273 A1	TASK CONCURRENCY MANAGEMENT DESIGN METHOD	20071018	716/2	
US 20070244676 A1	Adaptive analysis methods	20071018	703/2	
US 20070234257 A1	Method and Apparatus for Circuit Partitioning and Trace Assignment in Circuit Design	20071004	716/7	
US 20070233918 A1	Data Communication Method and Apparatus Utilizing Credit-Based Data Transfer Protocol ar	20071004	710/100	
US 20070233598 A1	Providing payment software application as enterprise services	20071004	705/40	
US 20070225959 A1	Mechanism for estimating and controlling di/dt-induced power supply voltage variations	20070927	703/15	
US 20070219771 A1	Branching and Behavioral Partitioning for a VLIW Processor	20070920	703/15	
US 20070204252 A1	Methods and Systems for Placement	20070830	716/10	
US 20070200608 A1	Self-timed thermally-aware circuits and methods of use thereof	20070830	327/261	
US 20070200193 A1	Component arrangement and method for determining the temperature in a semiconductor coı	20070830	257/469	

US 20070198971 A1	Reconfigurable processing	20070823	717/140
US 20070198211 A1	Selection of wavelengths for integrated circuit optical metrology	20070823	702/159
US 20070186204 A1	Automatic back annotation of a functional definition of an integrated circuit design based upo	20070809	716/18
US 20070186199 A1	Heuristic clustering of circuit elements in a circuit design	20070809	716/7
US 20070165035 A1	DEFERRED SHADING GRAPHICS PIPELINE PROCESSOR HAVING ADVANCED FEATUR	20070719	345/506
US 20070162887 A1	Method of fabricating photo mask	20070712	716/21
US 20070162531 A1	Flow transform for integrated circuit design and simulation having combined data flow, contro	20070712	708/200
US 20070162268 A1	Algorithmic electronic system level design platform	20070712	703/14
US 20070157137 A1	METHOD AND APPARATUS FOR RETROFITTING SEMICONDUCTOR CHIP PERFORMAN	20070705	716/4
US 20070150846 A1	Methods and Systems for Placement	20070628	716/8
US 20070129926 A1	Hardware acceleration system for simulation of logic and memory	20070607	703/15
US 20070129924 A1	Partitioning of tasks for execution by a VLIW hardware acceleration system	20070607	703/14
US 20070124707 A1	Method and apparatus for facilitating variation-aware parasitic extraction	20070531	716/4
US 20070122785 A1	Interactive Education System for Teaching Patient Care	20070531	434/272
US 20070120239 A1	METHOD AND APPARATUS FOR FULL-CHIP THERMAL ANALYSIS OF SEMICONDUCTOI	20070531	257/684
US 20070118349 A1	Generation and use of integrated circuit profile-based simulation information	20070524	703/13
US 20070101310 A1	Model of sensitivity of a simulated layout to a change in original layout, and use of model in p	20070503	716/21
US 20070087756 A1	MULTIFACTORIAL OPTIMIZATION SYSTEM AND METHOD	20070419	455/450
US 20070079065 A1	Advanced dynamic disk memory module	20070405	711/113
US 20070078639 A1	FACILITATING SIMULATION OF A MODEL WITHIN A DISTRIBUTED ENVIRONMENT	20070405	703/17
US 20070078638 A1	Method for symbolic simulation of circuits having non-digital node voltages	20070405	703/14
US 20070067747 A1	Substrate noise tool	20070322	716/5
US 20070067545 A1	Data Communication Method and Apparatus Utilizing Credit-Based Data Transfer Protocol ar	20070322	710/310
US 20070067104 A1	Devices, methods, and systems for managing route-related information	20070322	701/211
US 20070061124 A1	Method for the creation of a hybrid cycle simulation model	20070315	703/16
US 20070053576 A1	Phase shifting test mask patterns for characterizing illumination and mask quality in image fo	20070308	382/144
US 20070053513 A1	INTELLIGENT ELECTRONIC APPLIANCE SYSTEM AND METHOD	20070308	380/201
US 20070044079 A1	A system and method for compiling a description of an electronic circuit to instructions adapt	20070222	717/136
US 20070038790 A1	Integrated circuit devices, methods, and computer program products for monitoring a bus	20070215	710/113
US 20070022402 A1	System and method for lithography simulation	20070125	716/21
US 20070016476 A1	INTERNET APPLIANCE SYSTEM AND METHOD	20070118	705/14
US 20070005842 A1	SYSTEMS AND METHODS FOR STALL MONITORING	20070104	710/62
US 20070005329 A1	Building integrated circuits using a common database	20070104	703/19
US 20070005321 A1	Building integrated circuits using logical units	20070104	703/14
US 20060282246 A1	METHODOLOGY FOR IMAGE FIDELITY VERIFICATION	20061214	703/13
US 20060277533 A1	Register and active element machines: commands, programs, simulators and translators	20061207	717/137
US 20060277509 A1	SYSTEM AND METHOD FOR ANALYZING POWER CONSUMPTION OF ELECTRONIC DE	20061207	716/5
US 20060275935 A1	Testing electromigration at multiple points of a single node	20061207	438/17
US 20060265577 A1	REAL-TIME MONITORING, ALIGNMENT, AND TRANSLATION OF CPU STALLS OR EVEN	20061123	712/244
US 20060259889 A1	Method and apparatus for extending processing time in one pipeline stage	20061116	716/10
US 20060259833 A1	METHOD OF TRANSLATING SYSTEM EVENTS INTO SIGNALS FOR ACTIVITY MONITOR	20061116	714/47

US 20060259774 A1	WATERMARK COUNTER WITH RELOAD REGISTER	20061116	713/176
US 20060259751 A1	MONITORING OF MEMORY AND EXTERNAL EVENTS	20061116	712/227
US 20060259664 A1	REAL-TIME PRIORITIZATION OF STALL OR EVENT INFORMATION	20061116	710/40
US 20060259431 A1	Apparatus and method for content protection using one-way buffers	20061116	705/51
US 20060247909 A1	System and method for emulating a logic circuit design using programmable logic devices	20061102	703/23
US 20060241930 A1	SIMULATION OF A PCI DEVICE'S MEMORY-MAPPED I/O REGISTERS	20061026	703/24
US 20060241909 A1	System review toolset and method	20061026	702/183
US 20060236275 A1	Method for determining relevant circuit parts in a circuit in the event of loading with a tempora	20061019	716/4
US 20060229929 A1	System and method for software development	20061012	705/9
US 20060218593 A1	Digital coaxial cable LAN	20060928	725/74
US 20060200785 A1	Method and apparatus for the design and analysis of digital circuits with time division multiple	20060907	716/6
US 20060200260 A1	System and method for intermachine markup language communications	20060907	700/86
US 20060200259 A1	Network media appliance system and method	20060907	700/86
US 20060200258 A1	Vehicular information system and method	20060907	700/86
US 20060200253 A1	Internet appliance system and method	20060907	700/19
US 20060190634 A1	Computer chip set having on board wireless on board wireless interfaces to support parallel c	20060824	710/15
US 20060179182 A1	Data communication method and apparatus utilizing programmable channels for allocation o	20060810	710/29
US 20060176851 A1	Computer chip set having on board wireless interfaces to support test operations	20060810	370/331
US 20060174158 A1	Internal data bus interconnection mechanism utilizing central interconnection module converti	20060803	714/10
US 20060174050 A1	Internal data bus interconnection mechanism utilizing shared buffers supporting communicati	20060803	710/310
US 20060174040 A1	Data communication method and apparatus utilizing credit-based data transfer protocol and	20060803	710/29
US 20060161875 A1	Method of creating core-tile-switch mapping architecture in on-chip bus and computer-readab	20060720	716/14
US 20060155398 A1	Adaptive pattern recognition based control system and method	20060713	700/86
US 20060149527 A1	System and method to determine peak power demand in an integrated circuit	20060706	703/18
US 20060148429 A1	Transmission path simulation method and transmission path simulator	20060706	455/115.1
US 20060136653 A1	Systems and methods for exposing processor topology for virtual machines	20060622	711/6
US 20060129370 A1	Inter integrated circuit extension via shadow memory	20060615	703/20
US 20060123365 A1	Power managers for an integrated circuit	20060608	716/4
US 20060117274 A1	Behavior processor system and method	20060601	716/1
US 20060110837 A1	Method and system for topography-aware reticle enhancement	20060525	438/14
US 20060107120 A1	Microprocessor design support for computer system and platform validation	20060518	714/37
US 20060100840 A1	Mechanism for estimating and controlling di/dt-induced power supply voltage variations	20060511	703/18
US 20060095894 A1	Method and apparatus to provide graphical architecture design for a network processor havin	20060504	717/113
US 20060095879 A1	Method and apparatus to estimate delay for logic circuit optimization	20060504	716/6
US 20060095876 A1	Method and apparatus for full-chip thermal analysis of semiconductor chip designs	20060504	716/4
US 20060095872 A1	Integrated circuit devices and methods and apparatuses for designing integrated circuit devic	20060504	716/1
US 20060095870 A1	Power network analyzer for an integrated circuit design	20060504	716/1
US 20060092162 A1	Scalable high performance 3D graphics	20060504	345/506
US 20060080076 A1	System-level power estimation using heteregeneous power models	20060413	703/18
US 20060072014 A1	Smart optical sensor (SOS) hardware and software platform	20060406	348/159
US 20060059387 A1	Processor condition sensing circuits, systems and methods	20060316	714/30

US 20060059253 A1	Architectures for netcentric computing systems	20060316	709/223
US 20060053401 A1	Methods and apparatuses for designing integrated circuits	20060309	716/11
US 20060053246 A1	Systems and methods for providing nonvolatile memory management in wireless phones	20060309	711/100
US 20060052994 A1	Simulation system, simulation method and simulation program for verifying logic behavior of	20060309	703/14
US 20060031794 A1	Method and apparatus for thermal modeling and analysis of semiconductor chip designs	20060209	716/4
US 20060031357 A1	Method of and system for management of electronic mail	20060209	709/206
US 20060004557 A1	System and method for reducing size of simulation value change files	20060105	703/14
US 20050283756 A1	Method and system to automatically generate performance evaluation code for multi-threade	20051222	717/109
US 20050283349 A1	Design method, design program, and storage medium for semiconductor integrated device	20051222	703/14
US 20050278702 A1	Modeling language and method for address translation design mechanisms in test generation	20051215	717/124
US 20050278680 A1	Methodology for scheduling, partitioning and mapping computational tasks onto scalable, hig	20051215	716/16
US 20050278157 A1	System and method for simulating human movement using profile paths	20051215	703/6
US 20050276329 A1	Method and apparatus for performing motion compensation on video data	20051215	375/240.16
US 20050268258 A1	Rule-based design consultant and method for integrated circuit design	20051201	716/4
US 20050261884 A1	Unified modeling language (UML) design method	20051124	703/13
US 20050261859 A1	Systems and methods for evaluating a test case	20051124	702/120
US 20050257078 A1	System and method of workload-dependent reliability projection and monitoring for microproc	20051117	714/1
US 20050240895 A1	Method of emulation of lithographic projection tools	20051027	716/19
US 20050240887 A1	Generating test patterns having enhanced coverage of untargeted defects	20051027	716/4
US 20050234692 A1	Logic design modeling and interconnection	20051020	703/13
US 20050228630 A1	VCD-on-demand system and method	20051013	703/19
US 20050223190 A1	Hardware functional partitioning in a system platform of a telecommunication network elemer	20051006	712/13
US 20050193359 A1	Method and apparatus for designing circuits using high-level synthesis	20050901	716/18
US 20050192787 A1	Simulation apparatus and method of designing semiconductor integrated circuit	20050901	703/18
US 20050188009 A1	High-availability super server	20050825	709/203
US 20050166174 A1	System and method for lithography simulation	20050728	716/20
US 20050166168 A1	Method and apparatus for retrofitting semiconductor chip performance analysis tools with full	20050728	716/6
US 20050166166 A1	Method and apparatus for thermal testing of semiconductor chip designs	20050728	716/4
US 20050165597 A1	Apparatus and method for performing hardware and software co-verification testing	20050728	703/27
US 20050156165 A1	Test assembly including a test die for testing a semiconductor product die	20050721	257/48
US 20050151562 A1	Apparatus and method for bus signal termination compensation during detected quiet cycle	20050714	326/30
US 20050128489 A1	Parametric optimization of optical metrology model	20050616	356/601
US 20050122500 A1	System and method for lithography simulation	20050609	355/67
US 20050120327 A1	System and method for lithography simulation	20050602	716/20
US 20050120012 A1	Adaptive hierarchy usage monitoring HVAC control system	20050602	707/3
US 20050108667 A1	METHOD FOR DESIGNING AN INTEGRATED CIRCUIT HAVING MULTIPLE VOLTAGE DO	20050519	716/4
US 20050102125 A1	Inter-chip communication system	20050512	703/14
US 20050097500 A1	System and method for lithography simulation	20050505	716/20
US 20050094729 A1	Software and hardware partitioning for multi-standard video compression and decompression	20050505	375/240.16
US 20050091633 A1	System and method for lithography simulation	20050428	716/20
US 20050086565 A1	System and method for generating a test case	20050421	714/741

US 20050081170 A1	Method and apparatus for accelerating the verification of application specific integrated circuit	20050414	716/6
US 20050081130 A1	Using constrained scan cells to test integrated circuits	20050414	714/726
US 20050076322 A1	System and method for lithography simulation	20050407	716/20
US 20050076282 A1	System and method for testing a circuit design	20050407	714/739
US 20050071706 A1	Slew rate control mechanism	20050331	713/503
US 20050065762 A1	ESD protection device modeling method and ESD simulation method	20050324	703/14
US 20050057748 A1	Selecting a hypothetical profile to use in optical metrology	20050317	356/237.5
US 20050042527 A1	Phase shift mask including sub-resolution assist features for isolated spaces	20050224	430/5
US 20050039156 A1	Design method for essentially digital systems and components thereof and essentially digital	20050217	716/18
US 20050025054 A1	Extensible traffic generator for synthesis of network data traffic	20050203	370/235
US 20050015778 A1	Method and system for expressing the algorithms for the manipulation of hardware state usin	20050120	719/321
US 20050004774 A1	Methods and systems for inspection of wafers and reticles using designer intent data	20050106	702/108
US 20040268278 A1	Managing power on integrated circuits using power islands	20041230	716/5
US 20040252701 A1	Systems, processes and integrated circuits for rate and/or diversity adaptation for packet com	20041216	370/395.21
US 20040250150 A1	Devices, systems and methods for mode driven stops notice	20041209	713/330
US 20040249915 A1	Advanced multi-network client device for wideband multimedia access to private and public w	20041209	709/223
US 20040243959 A1	Design method for semiconductor integrated circuit device	20041202	716/7
US 20040236876 A1	Apparatus and method of memory access control for bus masters	20041125	710/22
US 20040236564 A1	Simulation of a PCI device's memory-mapped I/O registers	20041125	703/25
US 20040214150 A1	Interaction education system for teaching patient care	20041028	434/273
US 20040209169 A1	Method of Verifying the Placement of Sub-Resolution Assist Features in a Photomask Layout	20041021	430/5
US 20040204928 A1	Simulator apparatus and related technology	20041014	703/13
US 20040193957 A1	Emulation devices, systems and methods utilizing state machines	20040930	714/30
US 20040193390 A1	Method and apparatus for rapid evaluation of component mismatch in integrated circuit perfo	20040930	703/2
US 20040193388 A1	Design time validation of systems	20040930	703/1
US 20040168044 A1	Input pipeline registers for a node in an adaptive computing engine	20040826	712/220
US 20040159700 A1	Method and apparatus for secure import of information into data aggregation program hosted	20040819	235/380
US 20040153301 A1	Integrated circuit development methodology	20040805	703/14
US 20040148151 A1	Model simulation and calibration	20040729	703/22
US 20040145033 A1	Integrated circuit devices and methods and apparatuses for designing integrated circuit devic	20040729	257/659
US 20040136587 A1	Method and device for determining the properties of an integrated circuit	20040715	382/145
US 20040133833 A1	Apparatus for selecting test patterns for logic circuit, computer implemented method for selec	20040708	714/738
US 20040131267 A1	Method and apparatus for performing quality video compression and motion estimation	20040708	382/236
US 20040130552 A1	Deferred shading graphics pipeline processor having advanced features	20040708	345/506
US 20040128416 A1	Apparatus and method for address bus power control	20040701	710/107
US 20040124874 A1	Apparatus and method for bus signal termination compensation during detected quiet cycle	20040701	326/30
US 20040123256 A1	Software traffic generator/analyser	20040624	716/4
US 20040117756 A1	Methods and apparatuses for designing integrated circuits	20040617	716/18
US 20040111327 A1	Product toolkit system and method	20040610	705/26
US 20040098687 A1	System and method for implementing a flexible top level scan architecture using a partitioning	20040520	716/7
US 20040088598 A1	Deskew architecture	20040506	713/503

US 20040078767 A1	Representing the design of a sub-module in a hierarchical integrated circuit design and analy:	20040422	716/8
US 20040068711 A1	Digital circuit synthesis including timing convergence and routability	20040408	716/18
US 20040054510 A1	System and method for simulating human movement	20040318	703/6
US 20040031058 A1	Method and apparatus for browsing using alternative linkbases	20040212	725/112
US 20040017575 A1	Optimized model and parameter selection for optical metrology	20040129	356/625
US 20040017574 A1	Model and parameter selection for optical metrology	20040129	356/625
US 20040012600 A1	Scalable high performance 3d graphics	20040122	345/506
US 20040010650 A1	Configurable multi-port multi-protocol network interface to support packet processing	20040115	710/305
US 20040004216 A1	Test assembly including a test die for testing a semiconductor product die	20040108	257/48
US 20040003362 A1	Timing abstraction and partitioning strategy	20040101	716/6
US 20030233504 A1	Method for detecting bus contention from RTL description	20031218	710/107
US 20030229900 A1	Method and apparatus for browsing using multiple coordinated device sets	20031211	725/87
US 20030229877 A1	System and method for configuring analog elements in a configurable hardware device	20031211	716/16
US 20030229482 A1	Apparatus and method for managing integrated circuit designs	20031211	703/14
US 20030226062 A1	System and method for testing response to asynchronous system errors	20031204	714/38
US 20030225535 A1	Selection of wavelengths for integrated circuit optical metrology	20031204	702/76
US 20030216901 A1	Design apparatus and a method for generating an implementable description of a digital syst	20031120	703/13
US 20030214326 A1	Distributed dynamically optimizable processing communications and storage system	20031120	326/101
US 20030212538 A1	Method for full-chip vectorless dynamic IR and timing impact analysis in IC designs	20031113	703/14
US 20030208728 A1	Method and system for simulating resist and etch edges	20031106	716/4
US 20030208350 A1	Facilitating simulation of a model within a distributed environment	20031106	703/22
US 20030204389 A1	Method for numerically simulating an electrical circuit	20031030	703/19
US 20030200425 A1	Devices, systems and methods for mode driven stops	20031023	712/229
US 20030200073 A1	Partitioning a model into a plurality of independent partitions to be processed within a distribu	20031023	703/17
US 20030196144 A1	Processor condition sensing circuits, systems and methods	20031016	714/34
US 20030192029 A1	System and method for software development	20031009	717/101
US 20030188299 A1	Method and apparatus for simulation system compiler	20031002	717/141
US 20030187853 A1	Distributed data storage system and method	20031002	707/10
US 20030187840 A1	Metrology diffraction signal adaptation for tool-to-tool matching	20031002	707/4
US 20030187602 A1	METROLOGY HARDWARE SPECIFICATION USING A HARDWARE SIMULATOR	20031002	702/94
US 20030172055 A1	Array transformation in a behavioral synthesis tool.	20030911	707/1
US 20030163295 A1	Generation and use of integrated circuit profile-based simulation information	20030828	703/14
US 20030154466 A1	Method and apparatus for compiling source code to configure hardware	20030814	717/138
US 20030149954 A1	Methods and apparatuses for designing integrated circuits	20030807	716/18
US 20030144828 A1	Hub array system and method	20030731	703/21
US 20030142819 A1	Device and method for evaluating algorithms	20030731	380/28
US 20030142726 A1	Universal rake receiver	20030731	375/146
US 20030139956 A1	Methods and systems for role analysis	20030724	705/7
US 20030128140 A1	Code compression algorithms and architectures for embedded systems	20030710	341/107
US 20030126059 A1	Intelectual property (IP) brokering system and method	20030703	705/36R
US 20030125923 A1	Simulation of di/dt-induced power supply voltage variation	20030703	703/20

US 20030125922 A1	Mechanism for estimating and controlling di/dt-induced power supply voltage variations	20030703	703/18
US 20030099252 A1	System for authorizing functionality in adaptable hardware devices	20030529	370/437
US 20030093764 A1	Automated system-on-chip integrated circuit design verification system	20030515	716/5
US 20030093255 A1	Hot plug and hot pull system simulation	20030515	703/13
US 20030093252 A1	Message packet logging in a distributed simulation system	20030515	703/13
US 20030088840 A1	Method of designing semiconductor integrated circuit device, method of analyzing power cons	20030508	716/7
US 20030079195 A1	Methods and apparatuses for designing integrated circuits	20030424	716/8
US 20030079132 A1	Computer functional architecture and a locked down environment in a client-server architectu	20030424	713/182
US 20030075765 A1	Semiconductor integrated circuit	20030424	257/393
US 20030073060 A1	Interactive education system for teaching patient care	20030417	434/262
US 20030037305 A1	Method and apparatus for evaluating logic states of design nodes for cycle-based simulation	20030220	716/4
US 20030018461 A1	Simulation monitors based on temporal formulas	20030123	703/14
US 20030016461 A1	Systems, apparatus, and methods to determine thermal decay characterization from an equa	20030123	360/25
US 20030013024 A1	Phase shift mask including sub-resolution assist features for isolated spaces	20030116	430/5
US 20030009734 A1	Method for generating design constraints for modules in a hierarchical integrated circuit desig	20030109	716/6
US 20030008222 A1	Phase shift mask layout process for patterns including intersecting line segments	20030109	430/5
US 20030007379 A1	Directional coupling memory module	20030109	365/52
US 20030005263 A1	Shared resource queue for simultaneous multithreaded processing	20030102	712/218
US 20020197546 A1	Phase shift masking for "double-T" intersecting lines	20021226	430/5
US 20020194572 A1	Methods and apparatuses for designing integrated circuits	20021219	716/1
US 20020186721 A1	Methods and systems for monitoring traffic received from and loading simulated traffic on brc	20021212	370/522
US 20020161907 A1	Adaptive multi-protocol communications system	20021031	709/230
US 20020152060 A1	Inter-chip communication system	20021017	703/17
US 20020151992 A1	Media recording device with packet data interface	20021017	700/83
US 20020149598 A1	Method and apparatus for adjusting subpixel intensity values based upon luminance characte	20021017	345/589
US 20020147875 A1	Response and data phases in a highly pipelined bus architecture	20021010	710/305
US 20020144247 A1	Method and apparatus for simultaneous optimization of code targeting multiple machines	20021003	717/155
US 20020144212 A1	System, method and computer program product for web-based integrated circuit design	20021003	716/1
US 20020144183 A1	Microprocessor design support for computer system and platform validation	20021003	714/37
US 20020138814 A1	Virtual component having a detachable verification-supporting circuit, a method of verifying th	20020926	716/5
US 20020133785 A1	Semiconductor integrated circuit manufacturing method and model parameter extracting metl	20020919	716/1
US 20020133325 A1	Discrete event simulator	20020919	703/17
US 20020124234 A1	Method for designing circuits with sections having different supply voltages	20020905	716/18
US 20020124085 A1	Method of simulating operation of logical unit, and computer-readable recording medium reta	20020905	709/226
US 20020123872 A1	Method and apparatus for simulating manufacturing, electrical and physical characteristics of	20020905	703/15
US 20020108092 A1	Digital circuit design method using programming language	20020808	716/1
US 20020099756 A1	Task concurrency management design method	20020725	718/102
US 20020097216 A1	Animated video device with synchronized voice	20020725	345/108
US 20020095304 A1	System, method, and apparatus for storing emissions and susceptibility information	20020718	705/1
US 20020091991 A1	Unified real-time microprocessor computer	20020711	717/106
US 20020087940 A1	Method for designing large standard-cell based integrated circuits	20020704	716/2

US 20020087939 A1	Method for designing large standard-cell based integrated circuits	20020704	716/2
US 20020087275 A1	Visualization and manipulation of biomolecular relationships using graph operators	20020704	702/19
US 20020073380 A1	Block based design methodology with programmable components	20020613	716/1
US 20020066082 A1	Bus performance evaluation method for algorithm description	20020530	717/135
US 20020059554 A1	Design method for semiconductor integrated circuit device	20020516	716/8
US 20020059501 A1	High-availability super server	20020516	711/144
US 20020040466 A1	Automated EMC-driven layout and floor planning of electronic devices and systems	20020404	716/9
US 20020039030 A1	System, method, and apparatus for product diagnostic and evaluation testing	20020404	324/750
US 20020038401 A1	Design tool for systems-on-a-chip	20020328	710/305
US 20020033706 A1	System method, and apparatus for field scanning	20020321	324/750
US 20020023252 A1	METHOD FOR INCREMENTAL TIMING ANALYSIS	20020221	716/6
US 20020022951 A1	Method, apparatus and computer program product for determination of noise in mixed signal	20020221	703/16
US 20020019969 A1	Hardware and software co-simulation including simulating the cache of a target processor	20020214	716/5
US 20020018526 A1	Data transmission system of directional coupling type using forward wave and reflection wave	20020214	375/257
US 20020016704 A1	Adjoint sensitivity determination for nonlinear circuit models	20020207	703/14
US 20020016674 A1	Golf course yardage and information system having improved zone information and display c	20020207	701/215
US 20020013918 A1	Devices, systems and methods for mode driven stops	20020131	714/30
US 20020011949 A1	Golf course yardage and information system with zone detection	20020131	342/357.06
US 20020010544 A1	Display monitor for golf cart yardage and information system	20020124	701/213
US 20020004927 A1	Method for designing ingegrated circuit	20020110	716/2
US 20010056341 A1	Method and apparatus for debugging programs in a distributed environment	20011227	703/22
US 20010049593 A1	Software tool to allow field programmable system level devices	20011206	703/14
US 20010039640 A1	Method and apparatus for wiring integrated circuits with multiple power buses based on perfo	20011108	716/2
US 20010037424 A1	Snoop phase in a highly pipelined bus architecture	20011101	710/220
US 20010037421 A1	Enhanced highly pipelined bus architecture	20011101	710/305
US 20010029601 A1	Semiconductor device analyzer, method for analyzing/manufacturing semiconductor device, a	20011011	716/19
US 20010012014 A1	SINGLE LOGICAL IN X WINDOWS WITH DIRECT HARDWARE ACCESS TO THE FRAME	20010809	345/541
US 20010011212 A1	METHOD AND APPARATUS FOR GATE-LEVEL SIMULATION OF SYNTHESIZED REGISTI	20010802	703/22